Study program:	**Electrical and computer engineering – Module: Computer engineering**
Type and level of studies:	**Undergraduate academic studies (first level of studies)**
Course unit:	**VLSI system design**
Teacher in charge:	**Uroš Pešović**
Language of instruction:	**English**
ECTS:	**6**
Prerequisites:	-
Semester:	**Winter**

Course unit objective
Introducing students to the design principles of computer VLSI systems. Knowledge of hardware description languages.

Learning outcomes of Course unit
Students are expected to develop the ability to design computer VLSI systems independently.

Course unit contents

Theoretical classes

Designing Computer VLSI Systems Using Hardware Description Languages: VHDL and VERILOG. Design principles of RISC processors on the design example of a single RISC processor: design stages, decision process. Prefabrication and postfabrication testing of components.

Practical classes

View a series of completed tasks. Examples of processor resource design and interconnections. Design, simulation and synthesis of a small but functional processor in FPGA technology.

Literature:

1.	Ashenden P., The Designer's Guide to VHDL, 3rd Edition, Morgan Kaufmann; 2008

Number of active teaching hours

Lectures:	Practice:	Other forms of classes:	Other classes	Independent work:
2	2	0		Case study:

Teaching methods:
Lectures, tutorials, projects, demonstrations

Examination methods (maximum 100 points)

Exam prerequisites	**No. of points:**	**Final exam**	**No. of points:**
Student's activity during lectures		oral examination	20
Practical classes		written examination	40
Colloquiums			
Seminars/homework	40		

Grading system

Grade	**No. of points:**	**Description**
10	**91-100**	Excellent
9	**81-90**	Exceptionally good
8	**71-80**	Very good
7	**61-70**	Good
6	**51-60**	Passing
5	**less than 50**	Failing